IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Viterbi decoder for decoding a received sequence of data symbols which are coded using a predetermined coding instruction, and are transmitted via a transmission channel, having:

(a) a branch metric calculation circuit for calculation of branch metrics for the received sequence of coded data symbols;

(b) a path metric calculation circuit for calculation of path metrics and decision values as a function of the branch metrics and the coding instruction, with the calculated path metrics in each case being compared with an adjustable decision threshold value in order to produce an associated logic validity value, in which case the decision threshold value for the path metric normalization can be set such that it is variable;

(c) a selection circuit which temporarily stores only those path metrics whose validity value is logic high in a memory, and selects from the temporarily stored path metrics that path with the optimum path metric, with an increasing number of decision values being stored in the selection circuit as the signal-to-noise ratio of the transmission channel decreases.

(d) wherein two or more logic validity values which are produced by the path metric calculation circuit are logically OR-linked by a logic circuit, and all the associated decision values are temporarily stored in the memory of the selection circuit when the result of the logical OR linking is logic high.

2. (Previously Presented) Viterbi decoder according to Claim 1, wherein the selection circuit emits the data symbol sequence which is associated with the selected path for further data processing.

3. (Previously Presented) Viterbi decoder according to Claim 1, wherein the path metric calculation circuit sets the validity value of logic high when the associated calculated path metric is less than the threshold value.

4. (Previously Presented) Viterbi decoder according to claim 1, wherein the selection circuit selects the path with the lowest calculated path metric.

5. (Previously Presented) Viterbi decoder according to claim 1, wherein the path metric calculation circuit contains two or more path metric calculation elements.

6. (Previously Presented) Viterbi decoder according to claim 1, wherein a path metric calculation element in each case calculates the path metrics of two paths and compares them with one another, and emits the lower of the two path metrics to an associated clock memory element for temporary storage.

7. (Previously Presented) Viterbi decoder according to claim 1, wherein the path metric calculation element has:

(a) a first adder, which adds the branch metric of a first path and the metric of the first path which is temporarily stored in the associated clock memory element, and emits this to a first input of a multiplexer,

(b) a second adder, which adds the branch metric of a second path and the path metric of the second path which is temporarily stored in the associated clock memory element, and emits this to a second input of the multiplexer,

(c) a first comparator circuit, which compares the sum values calculated by the two adders, with the comparison result being emitted as a decision value to the selection circuit and to the multiplexer as a control signal, with the multiplexer passing on the lower of the sum values calculated by the two adders to the associated clock register;

(d) a second comparator circuit, which compares the passed-on sum value with the adjustable decision threshold value and emits a logic high validity value when the passed-on sum value is less than the decision threshold value.

8. (Previously Presented) Viterbi decoder according to claim 1, wherein the adjustable decision threshold value is a power value to the base two.

9. (Canceled)

10. (Previously Presented) Viterbi decoder according to claim 1, wherein the path metrics are calculated sequentially by the path metric calculation elements.

11. (Currently Amended) Viterbi decoder according to claim 1, wherein a number of path metrics, which correspond to the number N_{TS} of states in a ~~trellis~~ Trellis diagram, are calculated using 2^K path metric calculation elements, and in that the number 2^K of calculation element is given by:

$$1 \leq 2^K \leq \frac{N_{TS}}{2} .$$

12. (Previously Presented) Viterbi decoder according to Claim 11, wherein the path metric calculation elements are butterfly calculation elements, and in that the number 2^K of calculation element is given by:

$$1 \leq 2^K \leq \frac{N_{TS}}{2} .$$

13. (Previously Presented) Viterbi decoder according to Claim 12, wherein the path metric calculation elements are add-compare calculation elements, and in that the number 2^K of calculation element is given by:

$$1 \leq 2^K \leq N_{TS}.$$

14. (Currently Amended) Viterbi decoder according to claim 1, wherein the coding instruction is a ~~trellis~~ Trellis code, which has 2^L state transitions, where

$$0 \leq L < \infty$$

and L is a natural number.

15. (Currently Amended) Viterbi decoder according to Claim 11, wherein the ~~trellis~~ Trellis code has two state transitions.

16. (Currently Amended) Method for decoding a coded sequence of data symbols which are coded using a predetermined coding instruction, having the following steps:

(a) reception of the coded data symbol sequence via a transmission channel;

(b) calculation of branch metrics for the received data symbol sequence;

(c) calculation of path metrics and decision values for the received data symbol sequence as a function of the branch metrics and the coding instruction;

(d) comparison of the calculated path metrics with a decision threshold value for production of logic validity values, in which case the decision threshold value for path metric normalization can be set such that it is variable;

(e) storage of those calculated path metrics whose validity values are logic high in a temporary store, with an increasing number of decision values being stored as the signal-to-noise ratio of the transmission channel decreases, wherein two or more produced logic validity values are logically OR-linked and all the associated decision values are temporarily stored in the temporary store when the result of the logical OR linking is high;

(f) selection of that path whose stored path metric is a minimum;

(g) determination of the data symbol sequence associated with the selective path, by means of the coding instruction;

(h) emission of the determined data symbol sequence for further data processing.